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| 10 053,160      | 01.15.2002  | Tsai-Yu Huang        | B-4453 619445-9     | 1875             |

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Richard P. Berg, Esq.  
c/o LADAS & PARRY  
Suite 2100  
5670 Wilshire Boulevard  
Los Angeles, CA 90036-5679

EXAMINER

VINH, LAN

ART UNIT PAPER NUMBER

1765

DATE MAILED: 04.18.2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.

Applicant(s)

10/053 160

HUANG ET AL

## Office Action Summary

Examiner

Art Unit

Lan Vinh

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 05 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7 and 8 is/are rejected.
- 7) ☒ Claim(s) 6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- 1 ☐ Certified copies of the priority documents have been received.
- 2 ☒ Certified copies of the priority documents have been received in Application No. 10/053160.
- 3 ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Dunne et al (US 6,207,583)

Dunne discloses a photoresist ashing process comprising the steps of:

forming a hardmask layer 40 on a layer 38 (col 8, lines 53-54, fig.5(b) ), which reads on forming a mask layer on a semiconductor substrate

forming a patterned photoresist layer 42 on the surface of hardmask/mask layer 40 (col 8, lines 45-46)

forming a conformal layer 43 on the surface of the patterned photoresist layer 42 . layer 43 is removed subsequently (col 8, lines 47-51, fig. 5(b)), which reads on forming a victim layer on the surface of the photoresist according to the photoresist topography. the thickness of layer 43 is thinner than that of photoresist 42 as shown in fig.5(b). fig.5(b) also shows that a plurality of slopes are formed on the sidewalls of the patterned photoresist 42

etching the hardmask layer 40 using the patterned photoresist pattern and layer 43 as the mask (col 8, lines 48-50, fig. 5(b))

3. Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Dunne et al (US 6,207,583)

Dunne discloses a photoresist ashing process comprising the steps of:

forming an integrated circuit having a substrate, the substrate has metal lines on one or both substrate surfaces (col 4, lines 49-57), which reads on providing a semiconductor with semiconductor elements or inner leads on the surface

forming a hardmask layer 40 over the substrate (col 8, lines 53-54, fig.5(b) ), which reads on forming a protecting layer on the inner leads

forming a patterned photoresist layer 42 on the surface of hardmask/protecting layer 40 (col 8, lines 45-46)

forming a conforming layer 43 on the surface of the patterned photoresist layer 42 , layer 43 is removed subsequently (col 8, lines 47-51, fig. 5(b)), which reads on forming a victim layer on the surface of the photoresist according to the photoresist topography, the thickness of layer 43 is thinner than that of photoresist 42 as shown in fig.5(b), fig 5(b) also shows that a plurality of slopes are formed on the sidewalls of the patterned photoresist 42

etching the hardmask layer/protecting layer 40 using the patterned photoresist pattern and layer 43 as the mask to form a plurality of vias /windows connecting to the  
col 8, lines 48-50, fig. 5(b) which reads on etching the protecting layer

to form a plurality of metal contacting windows using the photoresist and layer 43 as the mask.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunne et al (US 6,207,583) in view of Wang et al (US 6,291,887)

Dunne's method has been described above. Unlike the instant claimed inventions as per claims 2, 5, Dunne fails to disclose using nitride as a mask/protecting layer.

However, Wang discloses a method for forming a dual damascene structure comprises the step of forming a hardmask/mask/protecting layer 20 of silicon nitride (col 6, lines 12-13)

Since Dunne discloses forming a hardmask layer, one skilled in the art would have found it obvious to modify Dunne method by forming a nitride hardmask/mask layer in view of Wang teaching because according to Wang hardmask layer of silicon nitride serves to selectively protect the underlying layer during the etching step (col 6, lines 13-15)

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6. Claims 3, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunne et al (US 6,207,583) in view of Liu et al (US 5,972,773)

Dunne's method has been described above. Unlike the instant claimed inventions as per claims 3, 7, Dunne fails to disclose that the thickness of the conforming layer 43/victim layer is 800-1000 Angstroms.

However, Liu discloses a method for fabricating an integrated circuit comprises the steps of forming a thin conformal coating layer 24 on the patterned resist 16, the layer 24 has a thickness of 100-1000 Angstroms (col 3, lines 29-47), which reads on forming a victim layer having a thickness of 800-1000 Angstroms on the photoresist

Since Dunne discloses forming a hardmask layer/mask layer, one skilled in the art would have found it obvious to modify Dunne's method by forming a conformal layer having a thickness/victim layer having a thickness as per Liu because according to Liu a thickness of a thin layer, applied over the masking layer, is preferably about 100-1000 Angstroms (col 5, lines 41-50)

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dunne et al (US 6,207,583) in view of Hsiao et al (US 5,985,765)

Dunne's method has been described above. Unlike the instant claimed invention as per claim 8, Dunne fails to disclose that the plurality of metal contact windows/via are pad and fuse regions.

However, Hsiao discloses a method for reducing pad loss comprises the step of etching contact openings/windows to form bonding pad and fuse region on the substrate (col 5, lines 49-51)

Since Dunne discloses the step of etching contact vias using a mask, one skilled in the art would have found it obvious to employ Dunne's etching step to form pad and fuse region in view of Hsiao's teaching because Hsiao teaches that it is also common practice in the semiconductor industry to etch the bonding pad openings in the fuse openings using the same masking step to reduce manufacturing cost (col 1, lines 55-58)

***Allowable Subject Matter***

8. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: No prior art of record discloses forming an anti-reflective coating layer on the surface of the photoresist according to the photoresist topography. The closest prior art of Schrems (US 6,040,211) discloses forming a photoresist layer over the anti-reflective coating layer that is formed over a hardmask (col 4, lines 40-43)

***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.



LV  
April 16, 2003